CLAIMS

1. A decoder for simultaneously displaying a plurality of video sequences, said decoder comprising:

a controller for executing a plurality of instructions;

a memory for storing the plurality of instructions, wherein said plurality of instructions cause the controller to perform operations comprising:

receiving at least one compressed frame from each of a plurality of video sequences;

locating at least a past prediction frame in a memory for each of the plurality of video sequences;

decoding the at least one compressed frame from each of the plurality of video sequences from the past prediction frame for each of the plurality of video sequences; and

indicating a new past prediction frame and a new future prediction frame for each of at least one of the plurality of video sequences.

2. The decoder of claim 1, wherein the compressed frame comprises a picture.

3. The decoder of claim 1, wherein the decoding the at least one compressed frame from each of the plurality of video sequences occurs during one frame display period.

4. The decoder of claim 1, wherein the operations further comprise:

indicating a frame to be displayed for each of the plurality of video sequences.

5. The decoder of claim 4, wherein the frame to be displayed for each of the plurality of video sequences further comprises a frame selected from a group consisting of the decoded at least one compressed frame from the video sequence, or the new past prediction frame for the video sequence.

6. A method for simultaneously displaying a plurality of video sequences, said method comprising:

receiving at least one compressed frame from each of a plurality of video sequences;

locating at least a past prediction frame in a memory for each of the plurality of video sequences;

decoding the at least one compressed frame from each of the plurality of video sequences from the past prediction frame for each of the plurality of video sequences; and

indicating a new past prediction frame and a new future prediction frame for each of at least one of the plurality of video sequences.

7. The method of claim 6, wherein the compressed frame comprises a picture.

8. The method of claim 6, wherein the decoding the at least one compressed frame from each of the plurality of video sequences occurs during one frame display period.

9. The method of claim 6, further comprising:

indicating a frame to be displayed for each of the plurality of video sequences.

10. The method of claim 9, wherein the frame to be displayed for each of the plurality of video sequences further comprises a frame selected from a group consisting of the decoded at least one compressed frame from the video sequence, or the new past prediction frame for the video sequence.

11. A circuit for simultaneously displaying a plurality of videos, said circuit comprising:

a plurality of frame buffers for each storing an frame from each of said plurality of videos;

a first register for storing a plurality of indicators, each of said plurality of indicators associated with a particular one of the plurality of videos, and wherein each of said plurality of indicators referring to a particular one of the frame buffers; and

a display engine for presenting the plurality of videos, wherein the video engine simultaneously presents a frame from each frame buffer indicated by said plurality of indicators.

12. The circuit of claim 11, wherein the plurality of videos comprises four videos and wherein the plurality of frame buffers further comprises four frame buffers.

13. The circuit of claim 11, wherein each of the plurality of frame buffers further comprise:

a plurality of sub-buffers, each of the sub-buffers for storing a particular frame from a particular one of the plurality of videos.

14. The circuit of claim 11, further comprising a decoder for decoding each of said plurality of videos.

15. The circuit of claim 14, further comprising:

a second register for storing a plurality of indicators, wherein each of the indicators are associated with a particular one of the plurality of videos, and

wherein each of the indicators refer to a particular one of the buffers; and

wherein the decoder decodes a frame from a particular one of the plurality of videos by motion predicting from another frame stored in the frame buffer indicated by the indicator associated with the particular one of the plurality of videos in the second register.

16. The circuit of claim 15, further comprising:

a third register for storing a plurality of indicators, wherein each of the indicators are associated with a particular one of the plurality of videos, and wherein each of the indicators refer to a particular one of the buffers; and

wherein the decoder decodes a frame from a particular one of the plurality of videos by motion predicting from another frame stored in the frame buffer indicated by the indicator associated with the particular one of the plurality of videos in the third register.